REMARKS

Claims 1 – 14 and 16 remain pending in the present application. Amendments have been made to claims 1, 11 and 14 for clarification purposes. No new matter has been included thereby.

The Examiner has maintained his rejection of claim 1 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,355,527) in view of Wolf ("Silicon Processing for the VLSI ERA: Vol.2" Lattice Press, Sunset Beach, Ca., (1990), pp. 321 – 322). Here, the Examiner suggested that Lin et al. disclosed a method for forming split-gate flash memories with improved, increased coupling ratio and that Wolf, pp. 321 – 322, showed adjustment of channel threshold voltage using ion implantation. In the Response to Arguments in the Office Action dated June 18, 2003, the Examiner also stated,

> "With regard to Independent Claims 1 and 14, Examiner can only interpret language posed in limitations of claims and currently, Lin et al. discloses those tenets recited in the claims of the instant application of Applicant. There is no chronology of process steps disclosed in the reference or recited in the claims of the instant application. Therefore, arguments appear moot."

Applicants respectfully submit that the claims 1 and 14 as amended are patentable over the cited references. In particular, the amendment provides clarification to a certain chronology of steps that was indicated as lacking. Using claim 1 as an example, it now recites ion implantation into the common source region to precede the floating gate formation, such that a substantial portion of the floating gates overlies the implanted common source region in the substrate. Here, implanting ions occurs before forming the floating gates since a substantial portion of the floating gates overlies the implanted common source region. Logically and grammatically, forming the floating gates occurs after implanting ions in the manner claimed. In contrast, Lin et al. used a completely different process sequence. Column 6 lines 26 – 28 of Lin et al. stated, "source implantation is performed after the forming of the floating gate (140) as shown in FIG. 2E." Therefore, Claim 1 as amended clearly demonstrates a chronology of process

sequence that is different from the process sequence described in Lin et al. Wolf also failed to teach these claimed process steps.

The Examiner combined Lin et al. with Wolf to teach a concept of threshold voltage implanting. The combination of these references still fails to show or suggest the elements of claim 1. Claim 1 also recites that implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell, among other elements. Lin et al., however, suggested a completely different technique for providing a high coupling ratio. The increased coupling ratio of Lin et al. was provided by the introduction of a third polysilicon layer such that this additional poly line, through sidewall coupling, shares the voltage between the source and the floating gate (Col.1, lines 25 – 8, Col. 3, lines 57 – 61, Col. 4, lines 53 – 55, Col. 5, lines 21-25, Col 5, line 31 – 33). Although Wolf could have taught a generally concept of threshold voltage implanting, it failed to show or suggest that implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell in the manner claimed. Accordingly, claim 1 is patentable over the cited references.

The Examiner rejected claims 2 and 3 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above, and further in view of Sze ("Physics of Semiconductor Devices," John Wiley & Sons, New York (1981), p. 68). The Examiner rejected claim 4 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above, and further in view of Wolf et al. ("Silicon Processing for the VLSI ERA: Vol.1" Lattice Press, Sunset Beach, Ca., (1986), pp. 321 – 322). The Examiner also rejected claims 5 and 9 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above. The Examiner rejected claim 6 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 5 above. The Examiner rejected claim 7 under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 6 above, further in view of Mizuno ("Hot Carrier Injection Suppression Due to the Nitride-Oxide LDD Spacer Structure," IEEE Trans. On Electron Deices, Vol. 38, No. 3, (1991), pp. 584 – 591.) Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 6 above, and further in

view of Wilson ("Handbook of Multilevel Metallization for Integrated Circuits, " Noyes Publ., Westwood, New Jersey, (1993), p. 868). Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 6 above. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 4 above. Claims 12 ad 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 5 above.

The Applicants submit that dependent claims 2–13 that are dependant from the amended claim 1 are also patentable. The dependent claims are patentable at least for the reasons given above, among other reasons. Here, the cited references do not show or suggest the combination of elements included in claims 2 – 13 when combined with independent claim 1. As noted, these claims are also patentable for other reasons.

In particular, claim 3 is patentable over the cited art. Claim 3 further recites that the ions implanted to form the common source region include arsenic ions. The Examiner stated in the Response to Arguments in the Office Action dated June 18, 2003,

> "Arguments pertaining to enhanced vertical diffusion of phosphorus are irrelevant here, both from the viewpoint that the thermal budget is scant, and from the results of Lin et al. who showed an increase in coupling."

The Applicants would like to point out that the Examiner's statements include arguments that appear inconsistent. If the thermal budget is scant as noted by the Examiner, then diffusion is limited and cannot lead to increased coupling in Lin et al. between the floating gate and the source region. The Examiner's arguments are inconsistent-How could diffusion be limited and still increase coupling! Because coupling ratio from phosphorus source diffusion was limited, Lin et al. resorted to a completely different technique for providing a high coupling ratio. As noted before, Lin et al. proposed a third polysilicon layer to increase the coupling ratio. The Examiner also referred to Sze to indicate that diffusion coefficients of n-type dopants were well known and that phosphorus diffused faster than arsenic. It would then follow that using arsenic as indicated for source implant in Lin et al. would have decreased the coupling ratio. In fact, Lin et al. clearly taught away from using arsenic in source region implant. For example, Lin at al. stated (Col. 6 lines 42 – 44), "Source implant is accomplished,

preferably, by using phosphorous ions." In addition, even though claim 21 of Lin et al. suggested using arsenic for drain region implantation, claim 15 of Lin et al. clearly recited using phosphorus for source region implantation. Accordingly, the combination of Lin et al., Wolf, and Sze not only failed to show or suggest, but actually taught away from, the elements of claim 3 in the instant application, which recites that the ions implanted to form the common source region include arsenic ions. Therefore, claim 3 is patentable over the cited references.

Claim 11 is also patentable over the cited references. Claim 11 recites a method in which implanting ions into the substrate to form the common source region includes implanting arsenic ions at a dose in the range of 1×10^{14} /cm^2 to 5×10^{14}/cm^2 and at an energy range of 80 to 150 KeV. The Examiner combined Sze, Wolf and Lin et al. to reject claim 11 as unpatentable under 35 U.S.C. 103(a). However, as noted in the previous paragraph, the combination of Lin et al., Wolf, and Sze not only failed to show or suggest, but actually taught away from, using arsenic in the source region implant as recited in claim 11 in the instant application. Accordingly, claim 11 is patentable over the cited references.

Claims 14 has been rejected under 35 U.S.C 103(a) as being unpatentable over Lin et al. in view of Wolf, Mizuno et al., and Wilson et al. The Examiner indicated that Lin et al. suggested a method of forming high coupling ratio flash memory as recited in the instant application. In the Response to Arguments in the Office Action dated June 18, 2003, the Examiner also stated that there was no chronology of process steps disclosed in the reference or recited in the claims of the instant application. Applicants respectfully submit that the claim 14 has been amended for clarification purposes and demonstrate certain chronology. Claim 14 now recites each floating gate region having a substantial portion overlying the common source region which has a portion that has been implanted with the first ions. Here, implanting ions occurs before forming the floating gates since a substantial portion of the floating gates overlies the implanted portion of the common source region. Logically and grammatically, forming the floating gates occurs after implanting ions in the manner claimed. Lin et al. used a completely different process sequence. Column 6 lines 26 – 28 of Lin et al. clearly stated, "source

implantation is performed after the forming of the floating gate (140) as shown in FIG. 2E." Accordingly, claim 14 is patentable over Lin et al.

The Examiner combined Lin et al. with the threshold implants of Wolf, the nitride spacers of Mizuno et al., and the conductive tungsten layers of Wilson et al. to teach a flash memory cell with increased coupling ratio. Applicants assert that the combination of these references fails to show or suggest the claimed combination of elements for fabricating a flash memory device having a high coupling ratio recited in claims 14. As noted earlier, Lin et al. taught a different method of increasing the coupling ratio by using a third polysilicon layer, which has nothing to do with Claim 14 of the instant invention. Although Wolf could have taught a generally concept of threshold voltage implanting, the combination of Lin et al. and Wolf still failed to show or suggest the method recited in Claim 14 which includes patterning and etching nitride masking layer to expose at least one first portion and at least one second portion of the first polysilicon layer overlying a portion of the implanted common source region, and implanting ions into portions of the substrate defined by the first and second floating gate regions and including opposite extremities of said common source region, in order to adjust the threshold voltage of the flash memory device. Similarly, although Mizuno et al. may have indicated the general concept of nitride spacers and Wilson ct al. could have taught the general concept of using tungsten as a conductive layer, these references in conjunction with Lin et al. still failed to teach the combination of elements in claim 14, which includes, among other things, forming second gate oxide over the first gate oxide layer, over the nitride spacers and over the floating gate oxide layer, forming a second polysilicon layer over the second gate oxide layer, forming a conductive layer over the second polysilicon layer, and removing portions of the conductive layer, second polysilicon layer, second oxide layer, nitride spacers and first gate oxide layer to form a plurality of select gates having a portion overlying a portion of an associated one of the floating gates. It is clear that Lin et al. and the other cited references, taken either singly or collectively, failed to show or suggest the combination of claim elements of claim 14. Accordingly, claim 14 is also patentable over the cited references.

Claims 16 has been rejected under 35 U.S.C 103(a) as being unpatentable over Lin et al. in view of Wolf, Mizuno et al., and Wilson et al., as applied to Claim 14.

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Applicants respectfully disagree. Since claim 16 is dependant from independent claim 14, claim 16 is patentable for at least the reasons given above. Additionally, the cited references did not show or suggest the claim elements in claim 16, which recites that the first ions include N-type ions and the second ions include P-type ions. Therefore, claim 16 is patentable over the cited art.

Having thus amended the application for clarification and having established that the cited references, taken either singly or collectively, failed to show or suggest the combination of claim elements of the claims in the present application, Applicants respectfully submit that the application is in condition for allowance. It is respectfully requested that rejection of claims 1 – 14 and 16 be reconsidered, and early notice thereof is solicited

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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